Coplanar Waveguides and Microwave Inductors on Silicon Substrates

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Abstract— **Silicon has many advantages as a microwave substrate material including low cost and a mature technology. The aim of this paper is to evaluate the potential of using high-resistivity silicon as a low-cost low-loss microwave substrate through an experimental comparative study. Coplanar waveguides fabricated on Si, GaAs, and quartz substrates are tested and their characteristics are compared. Microwave spiral inductors and meander lines are also fabricated on various substrates, and their performance is also analyzed. The results demonstrate that the losses of a coplanar transmission line (CPW) realized on high-resistivity (3 k to 7 k Ω-cm) silicon substrates are comparable to the losses of a CPW realized on a GaAs substrate covered with insulators. Furthermore, measured unloaded Q's of microwave inductive structures on high-resistivity silicon substrates are comparable to the measured unloaded Q's of the same structures on GaAs and on quartz. This paper demonstrates that high-resistivity Si can be used as a microwave substrate.**

I. Introduction

HIGH COST is one of the problems of bringing high frequency personal communication equipment to the consumer market. Materials that provide superior microwave performance for the realization of active devices and passive elements are typically very expensive. Si offers many advantages as a microwave material and as a system substrate including:

- Silicon is a mature technology,
- It has an excellent planarity for all flip chip bumping and bonding technologies,
- It is a good thermal conductor,
- Multi-interconnect metal layers are easily achieved,
- An ample set of devices can be fabricated, and
- Devices that can not be fabricated on wafer can be realized on other materials and then flip chip attached.

The price of float zone silicon wafer has decreased considerably. Presently, a four-inch polished silicon wafer with bulk resistivity of 2 k Ω-cm costs $15.00. Five- and six-inch wafers are also available.

The MMIC concept started in 1964 [1] in an effort to reduce the size and weight of microwave transmitters and receivers. At that time, the microwave and the semiconductor technology [2] were in their infancies. The available technologies were: maximum Si resistivity was about 1600 Ω-cm, Si processing was poor (by today's standards), some aspects of semiconductor physics were not as well understood as they are now, microelectronics interconnects in a production environment were in the form of wire bond, and electrical interconnects were microstrip lines. Si substrates with resistivities greater than 1600 Ω-cm have been used in both theoretical [1], [9] and experimental investigations [10]. In [1], [3]–[10], the structure used for analysis was the microstrip line. In most cases, the loss analysis was done by considering metal and bulk semiconductor contributions. In none of the cases were Schottky (metal-semiconductor) junctions nor metal-insulator-semiconductor junctions considered. The microwave loss analysis was performed by considering the flatband voltage and the depletion width to be zero. Currently, both microwave and semiconductor technologies have matured. Several fabrication techniques have been developed, including submicron gate length transistor technologies, and flip-chip, and bump interconnects [11]. The semiconductor physics concepts are now well established [12]. Moreover, two- and three-dimensional electromagnetic analysis tools are well developed and can be obtained from several sources. Circuits in coplanar waveguide configurations are in products [13]. Uncompensated high-resistivity (HR) Si wafers are available at low cost. This certainly suggests that the potential of Si as a microwave substrate should be reassessed.

Previously, research has been performed on doped semiconductor substrates to realize slow-wave structures [14]–[16]. The aim was to control the substrate doping and carrier distributions to enhance the slow-wave phenomena. One should distinguish between this previous research and the work presented here. In the past, doped substrates, which slow the wave at the expense of increasing losses, were utilized. On the other hand, the aim of this paper is to demonstrate the potential of using HR silicon as a low-cost, low-loss microwave substrate.

In the next sections, experimental results will be presented to assess the performance of HR Si substrates in the microwave band. Coplanar waveguides fabricated on HR Si, semi-insulating (SI) GaAs, and quartz substrates are tested and their characteristics will be compared. Moreover, microwave inductive structures are also fabricated, and their performance will be analyzed as well.

II. Semiconductor Theoretical Background

The behavior of the semiconductor surface needs to be taken into account when realizing passive structures like

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transmission lines and inductors on semiconductor substrates, in particular, the metal-semiconductor and the metal-insulator-semiconductor interfaces.

When a metal is brought into contact with a semiconducting material, the surface of the semiconductor is depleted of carriers. The resistivity of the depleted region is very high. The depth of the depletion region width "W" and is given by

$$W = \sqrt{\frac{2\varepsilon_r \varepsilon_o \psi_o}{qN_b}} \tag{1}$$

where, ε_r is the dielectric constant of the semiconducting material, ε_o is the permittivity of vacuum, ψ_o is the built-in potential which is a function of the metallization system and of the semiconductor to which the metal system makes contact to, q is the magnitude of electron's charge, and N_b is the dopant concentration. The key parameter in (1) is the dopant concentration, which for standard Si is approximately 5×10^{16} (cm^{-3}) and for HR Si is approximately 10^{13} (cm^{-3}).

On the other hand, when a metal-insulator system is brought into contact with a semiconducting material, the surface of the semiconductor is filled with charges "Q_s." These charges at the surface can be: 1) accumulation charges (same as bulk type); 2) depletion charges; or, 3) inversion (opposite to bulk type) with depletion charges (small compared to inversion charges). The resistivity at the surface of the semiconductor decreases due to the presence of such charges. The semiconductor charges due to inversion are given by

$$Q_s(inversion) \approx -\frac{\varepsilon_r \varepsilon_o kT e^{\phi_s/2}}{L_{Di} q} \tag{2}$$

where, k is Boltzmann's constant, T is the temperature, ϕ_s is the surface potential, and L_{Di} is the intrinsic Debye length. The surface potential is given by

$$\phi_s = V_g - V_{FB} - \hat{U}_s \frac{\varepsilon_r \varepsilon_o kT F(U_s, U_F)}{C_{ox} q L_{Di}} \tag{3}$$

$$\hat{U}_s = \frac{U_s}{|U_s|},$$

$$U_s = \frac{q\phi_s}{kT},$$

$$U_F = \frac{q\phi_F}{kT} \tag{4}$$

$$F(U_s, U_F) = \sqrt{e^{U_F}(e^{-U_s} + U_s - 1) + e^{-U_F}(e^{U_s} - U_s - 1)} \tag{5}$$

where, V_g is the gate voltage, ϕ_F is the Fermi potential, and V_{FB} is the flat band voltage which is given by

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s = 0)}{C_{ox}} - \frac{1}{C_{ox}} \int_o^{x_o} \left(\frac{x}{x_o}\right) Q_m(x) dx. \tag{6}$$

In (4), ϕ_{ms} is the metal-semiconductor work function due to the metal semiconductor energy band difference, Q_f is the fixed charge density due primarily to structural defects in the insulator, Q_m is the mobile charge density due primarily to ionic impurities in the insulator, Q_{it} is the interface trapped charge density due to structural defects at the insulator semiconductor interface, and C_{ox} is the insulator(s) capacitance. The key parameter is the insulator capacitance C_{ox}, which is inversely proportional to the insulator thickness. For an MOS gate, the insulator thickness is about 150 Å. For the transmission lines and inductors in the MMIC technology under study, the insulator thickness is about 20,000 Å. Further definition of parameters and explanation of the usage and restrictions of (1)–(6) can be found in [17]–[19].

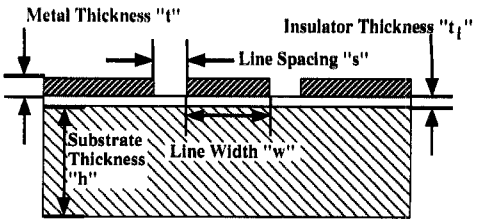

Fig. 1. Cross section of the CPW.

III. Si, GaAs, Quartz Substrates and the Realized Structures

The topology of the structures analyzed in this study can be divided into two groups. The first group consists of coplanar waveguides (CPW) on several substrates. A cross section of this structure is shown in Fig. 1. The second group consists of inductive structures, also on various substrates. Their cross section is shown in Fig. 2. The CPW and the inductive structure are chosen for the study due to their strong field interaction with the propagation medium. The cross section of the CPW and the inductors can be divided into two groups: metal-semiconductor and metal-insulator-semiconductor. Three main substrate materials are used in this comparative study, Si, GaAs, and quartz. The quartz substrate is used as a standard. Thin insulating layers are introduced in some structures between the substrate and the metallization layers, as shown in Fig. 2. These thin insulating layers are commonly used in MMIC process for the realization of MIM capacitors and the electric isolation between two metal layers. All the structures were processed under the same conditions [13] with the exception of SUB#6 which went first through a gate MOS oxide step. The geometries of interest are: metal thickness "t" (2.5 μm); substrate thickness "h" (quartz = 525 μm, Si = 400 μm, GaAs = 625 μm); and insulator thickness "t_i" as shown in Fig. 2. The structures are in a coplanar configuration. The CPW's line width "w" is 10 μm and line spacing "s" is 30 μm. Table I summarizes other properties of the structures including ground separation. A 12.7 μm diameter gold wire bond was used to connect the center of the single metal layer spiral inductor to its output. The spiral inductors have an outer diameter of 300 μm. The HR N type Si substrates have a (111) crystal orientation. The resistivity of the substrates were measured [20] before and after processing (not including the wafers where MOS gate oxide was grown). The resistivity remains constant in the range of 3000–7000 Ω-cm before and after processing which is in agreement with [21], and it is maintained as a function of substrate thickness.

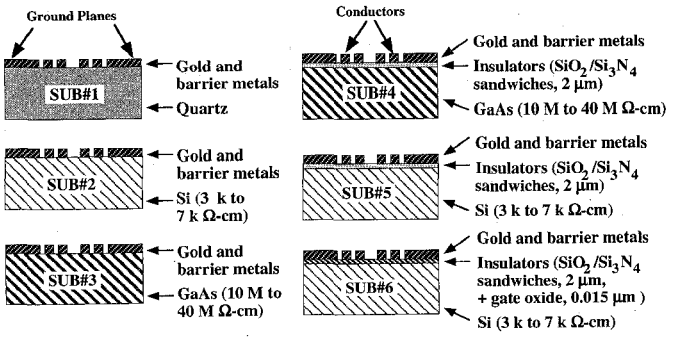

Fig. 2. Cross section of the fabricated structures.

TABLE I
SUMMARY OF STRUCTURES

Part	# Turns	Output Connection	Realized On Substrate #	Ground Separation (μm)	Line Length (μm)
CPW	---	---	1,2,4	---	1000
CPW	---	---	4,5,6	---	1400
Meander	---	---	1,2,3	30	---
Spiral	3	Wire Bond	1,2,3	25	---
Spiral	4	Wire Bond	1,2,3	25	---
Spiral	6	Underbridge	4,5,6	10	---

IV. MEASUREMENTS

The measurements were taken on wafer using: 1) HP 8510C Vector Network Analyzer; 2) CASCADE MICROTECH™ high frequency coplanar probes; 3) LRM calibration technique [22] to the probe tips; 4) a 6.35 mm quartz plate placed between the probe chuck and the sample to remove higher order modes of propagation.

For the CPW structures, a sample in each quadrant of the wafer was measured. The two port S parameter measurements were averaged and then translated into propagation constants using the Even and Odd mode method [23].

For the inductors, six samples were measured per structure to take into account process variability across the wafer. Measurement were taken as follows: two at center reticles and one at each of the 3, 6, 9, and 12 o'clock reticles located at the outer edge of the wafer. The two port S parameter measurements were averaged and then translated into a π-network. The unloaded input impedance of the π-network was then computed by leaving the output open. The unloaded Q was determined by dividing the imaginary part (inductive stored energy) by the real part (dissipated energy) of the unloaded input impedance. The unloaded Q was calculated only at the frequencies at which the imaginary part of the input impedance was linear (3 GHz for most structures under study).

A. Results and Discussions for CPW's Structures

The measured losses of the CPW shown in Fig. 3 realized on SUB#1 (quartz), SUB#2 (Si), and SUB#4 (GaAs with insulators) are presented in Fig. 4. Quartz with an effective dielectric constant (ε_{eff}) of 2.2 had the lowest losses when compared to Si with ε_{eff} of 5.7 or to GaAs substrate covered with insulators with ε_{eff} of 4.3. The dielectric constant

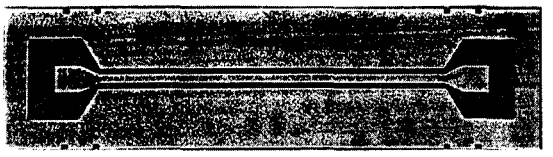

Fig. 3. CPW (line length = 1000 μm).

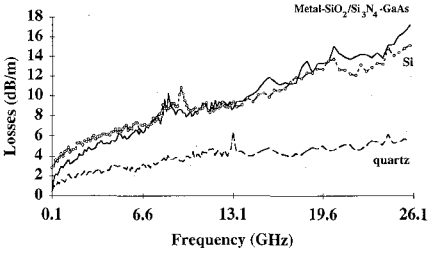

Fig. 4. CPW (line length = 1000 μm) measured losses versus frequency. For: SUB#2 (Si), Zo = 38 Ω, ε_{eff} = 5.7, ——o——; SUB#4 (GaAs cover with insulators), Zo = 38 Ω, ε_{eff} = 4.3, ——; SUB#1 (quartz), Zo = 61 Ω, ε_{eff} = 2.2, — — — —.

indicates the electric field concentration in the medium of propagation. The higher the dielectric constant, the higher the electric field concentration; therefore, the higher the current density at the edges of the transmission line. The three substrate losses on Fig. 4 are in agreement with this concept. However, around 7 GHz the losses of the SUB#4 became higher than those of SUB#2. This can be explained by loss mechanism of semiconductors. For bulk semiconductors, the loss is associated with the movement of majority carriers, known as ohmic loss, and with the internal polarization of the material when subjected to a time varying signal. Since the conduction due to majority carriers is constant as a function of frequency, the loss tangent due to ohmic loss varies inversely with frequency. In a semiconductor, the ohmic loss predominates [4] at low frequencies and the polarization loss dominates at high frequencies (Fig. 4).

The loss characteristics of the CPW on SUB#2 and SUB#4 can be explained by combining the above mentioned loss mechanisms with semiconductor theory. The depletion region width (1) of the metal-semiconductor junction increases with the substrate resistivity, thereby reducing the losses. Equation (1) is plotted in Fig. 5 as a function of the built-in potential for N and P types HR Si. According to Fig. 5, depletion widths of 20 μm can be obtained at 0.6 volt for N type 2 k Ω-cm Si substrates. When a metal-insulator system is brought into contact with a semiconductor surface an accumulation, a depletion, or an inversion region is formed depending on the surface potential. The semiconductor charge at the surface (2) is plotted as a function of the surface potential (3) in Fig. 6 for N and P types Si of low and HR, and GaAs. A MOS transistor is considered "ON" when the surface potential is $2\phi_f$. For the semiconductors plotted in Fig. 6:

Semiconductor	$2\phi_f$
GaAs-N (10 M Ω-cm)	−0.038 V
Si-N (10 k Ω-cm)	− 0.089 V
Si-N (2 k Ω-cm)	− 0.131 V
Si-P (0.33 Ω-cm)	0.778 V

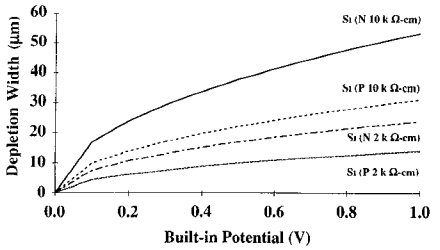

Fig. 5. Depletion width versus built-in potential for high resistivity silicon: N-type ρ = 2 k Ω-cm — - —; N-type ρ = 10 k Ω-cm - — - —; P-type ρ = 2 k Ω-cm - — - —; P-type ρ = 10 k Ω-cm - - - -.

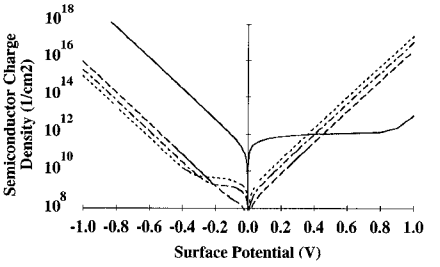

Fig. 6. Semiconductor charge density $|Qs|$ versus surface potential. Semiconductor, type, resistivity. Si, P, ρ = 0.33 Ω-cm ——; Si, N, ρ = 2 k Ω-cm - - - -; Si, N, ρ = 10 k Ω-cm — - —; GaAs, N, ρ = 10 M Ω-cm —— -.

The surface potential is a function of the flat band voltage which in turn depends on many parameters (3) including the metal-semiconductor work function difference, fixed charges, mobile charges, interface charges, and the insulator thickness. Even though the bulk resistivity of SUB#2 is between 3000 and 7000 Ω-cm, the surface resistivity (several microns into the substrate) is almost infinite. The majority of the field penetration of the CPW under study is within the first several microns.

Fig. 7 shows the measured losses for the CPW on SUB#5 which is realized on Si substrates with two microns of insulator. Here, the effect of the drop in the surface resistivity is clearly shown. The semiconductor-insulator interface is inverted or accumulated. The CPW on SUB#5 has almost an order of magnitude higher losses than the CPW on SUB#4 (GaAs substrate covered with insulators). One should notice that the surface states density in SI GaAs is orders of magnitude higher than Si. The surface states trap the inversion/accumulation charges from going to the conduction/valence band; therefore, the effective surface resistivity of Si is much lower than that of GaAs. The CPW on SUB#6 differs from the CPW on SUB#5 in that the silicon wafer was first processed through an MOS gate oxide growth (about 150 Å). The gate oxide growth reduces the mobile charges (Q_m) and the interface charges (Q_{it}). The charge reduction translates into a reduction of the flatband voltage according to (6) which further translates into the reduction of semiconductor charges at the surface (2 and 3). Even though two of the sources of flat band voltage are reduced, there is only a slight reduction in losses. This is due to the relationship between the charges and the metal-semiconductor capacitance which is reduced by adding the MOS gate oxide thickness which increases the effect of all the charges. Fig. 7 also indicates that the losses due to the semiconductor charges increased as the square root of frequency.

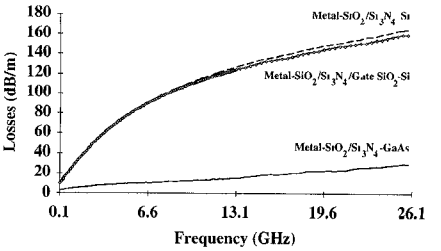

Fig. 7. CPW (line length = 1400 μm) measured losses versus frequency. For: SUB#4 (GaAs cover with insulators) ——; SUB#5 (Si cover with insulators) —— -; SUB#6 (Si cover with insulators including MOS gate oxide) —♦—.

B. Results and Discussions of the Microwave Inductive Structures

The measured results of CPW structures on HR Si substrate motivated further investigation in inductive structures. The cross sections are shown in Fig. 2. As expected, the inductors, shown in Figs. 8 and 9, fabricated on HR Si exhibited characteristics very similar to those on GaAs, and quartz substrates. The measured real and imaginary parts, shown in Figs. 10 and 11, respectively, of the unloaded input impedance of the meander inductor on SUB#1, SUB#2, and SUB#3 are comparable. At low frequencies, both the real and imaginary parts of the unloaded input impedance are indistinguishable from each other. Around 5 GHz the curves start to separate. The separation is due to the resonant characteristics of the structure. The differences in the curves in Figs. 10 and 11 at high frequency are attributed to the difference in the dielectric constant of the substrates. The inductors on GaAs resonate before those on Si and quartz due to the higher dielectric constant of the GaAs. There are no noticeable differences due to losses. Figs. 12–14 show the measured unloaded Q for the meander, the three turn spiral, and the four turn spiral inductors, respectively. As mentioned before, the Q is only calculated at the frequencies at which the structure can be used as an inductor and that is reason why the curves extend only to 3 GHz. The maximum value of Q, twice of the maximum shown, in the inductive structure under study is achieved in the frequency region of resonance. However, these are not reported because the inductive structures are not used at these frequencies due to the strong frequency dependence. The inductive structures on Si present unloaded Q factors that are very close to those of the other structures. This interesting result can be explained as follows: 1) The metal-semiconductor interface depletes the surface of the Si substrates of carriers; 2) the higher the resistivity, the wider [see Fig. 5, and (1)] the depletion region; and 3) the bulk of the electromagnetic field of the inductors is near the surface of the substrate.

The effect of a thin insulator layer between the metal and the substrate were also investigated in the inductive structures. Fig. 15 shows the real part of the input shunt admittance of the π-network of the six-turn spiral inductor realized on SUB#4, SUB#5, and SUB#6. The cross sectional views of these structures are shown in Fig. 2. Fig. 15 shows a similar pattern to that of Fig. 7. Here, as in the case of the CPW, a sharp difference between the GaAs and Si substrates is observed. When the insulator is introduced, a strong inversion or accumulation layer of charges is formed at the surface (see

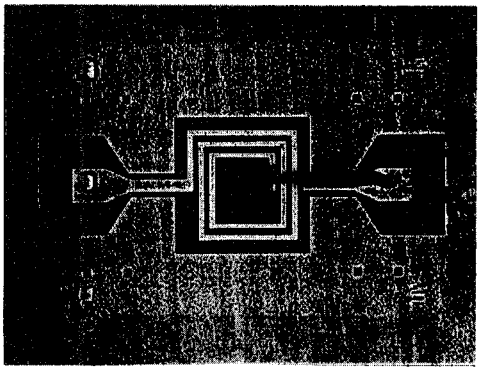

Fig. 8. Three-turn spiral inductor.

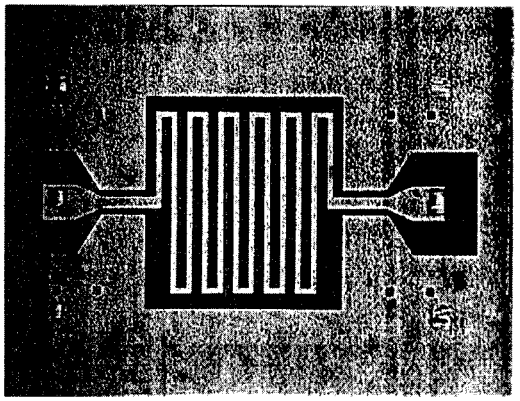

Fig. 9. Meander inductor.

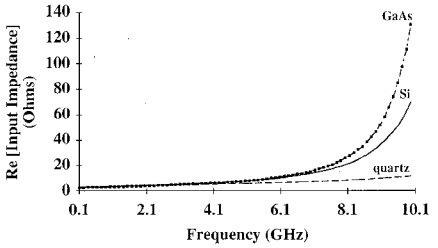

Fig. 10. Measured real part of unlocated input impedance (meander). SUB#1 (quartz) — - —; SUB#2 (Si) ——; SUB#3 (GaAs) —■—.

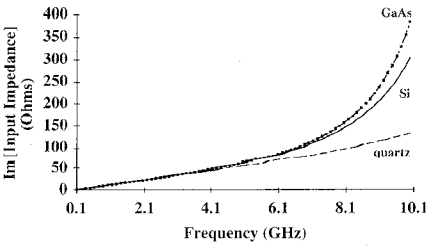

Fig. 11. Measured imaginary part of unloaded input impedance (meander). SUB#1 (quartz) — - —; SUB#2 (Si) ——; SUB#3 (GaAs) —■—.

Fig. 6) of the Si substrates. The MOS gate oxide process reduces the interface and mobile charges and decreases the metal-insulator-semiconductor capacitance. The end effect is a slight reduction in the accumulation/inversion charges at the surface; therefore, the input shunt losses are reduced. The losses due to the substrate inversion/accumulation charges

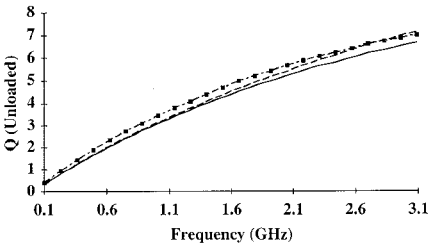

Fig. 12. Measured unloaded Q (meander). SUB#1 (quartz) — - —; SUB#2 (Si) ——; SUB#3 (GaAs) —■—.

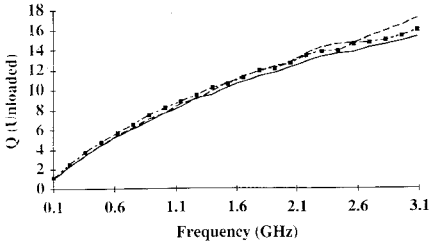

Fig. 13. Measured unloaded Q (three-turn spiral). SUB#1 (quartz) — - —; SUB#2 (Si) ——; SUB#3 (GaAs) —■—.

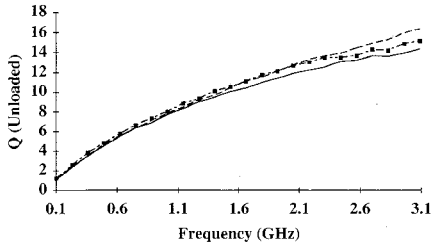

Fig. 14. Measured unloaded Q (four-turn spiral). SUB#1 (quartz) — - —; SUB#2 (Si) ——; SUB#3 (GaAs) —■—.

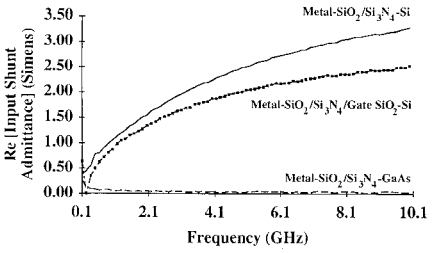

Fig. 15. Measured real part of π network input shunt admittance (six turn spiral). SUB#4 (GaAs cover with insulators) — - —; SUB#5 (Si cover with insulators) ——; SUB#6 (Si cover with insulators and MOS gate oxide) —■—.

increase as the square root of frequency. The substrate losses start to impact the device around 1 GHz. At 2 GHz, the unloaded Q, shown in Fig. 16, of the six spiral inductors on SUB#5 and SUB#6 (HR Si with insulators) is half that of SUB#4 (GaAs substrate covered with insulator). Figs. 15 and 16 explain why standard (i.e., below 30 Ω-cm) Si has been used to fabricate MMIC designs up to 2 GHz frequency region.

The lower Q of the six-turn spiral inductor compared to the three- and four-turn ones is attributed to 1) the ground plane is closer to the conductor, which leads to higher current density at the edges, 2) the losses of the under bridge metallization are higher than that of the wire bond, and 3) presence of inversion/accumulation charges.

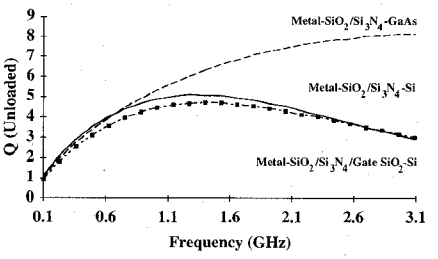

Fig. 16. Measured unloaded Q (six turn spiral). SUB#4 (GaAs cover with insulators) — - —; SUB#5 (Si cover with insulators) ——; SUB#6 (Si cover with insulators and MOS gate oxide) —■—.

V. Conclusion

The loss mechanisms of semiconductor substrates used for microwave applications were analyzed using both microwave and semiconductor physics concepts and were investigated experimentally. Si with measured resistivity between 3 k and 7 k Ω-cm produces transmission line losses on CPW comparable to that of GaAs substrate covered with insulators. Furthermore, the measured unloaded Q's of inductive structures on HR Si are comparable to the Q's of similar structures on GaAs and quartz substrates. These results demonstrate that HR Si can be used as a microwave substrate, which translates to lower-cost microwave products.

Acknowledgment

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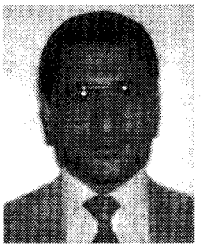

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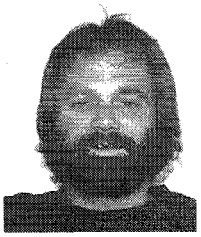

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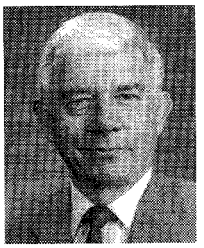
Mr. Dydyk was elected to Motorola's Science Advisory Board Associates (SABA) and awarded the Dan Noble Fellowship, Motorola's highest scientific honor. He has 26 patents to his credit with 11 pending and has published many papers in national technical journals.



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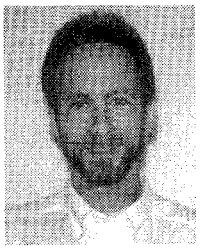
He joined the Westinghouse Research Labs in 1968 where he was engaged in research on various aspects of semiconductor devices, including MOS devices, imaging arrays, power devices, and magnetostatic waves. He spent a year at the Institute of Applied Solid State Physics in Germany during 1978. In 1981, he joined Arizona State University in the Center for Solid State Electronics Research. His current research interests are semiconductor materials and devices, photovoltaics, and defects in semiconductors. He has written two books *Advanced MOS Devices* and *Semiconductor Material and Device Characterization* and published more than 90 papers.



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